REMARKS

Claims 1-29 are currently pending in the subject application, and are presently under consideration. Claims 1-17 and 23 have been cancelled. Claims 18-21 and 25 stand rejected. Claims 22-24 and 26-29 are allowable. Claims 18-19, 21, 24 and 26-28 have been amended. Claims 30-42 have been added. Favorable reconsideration of the application is requested in view of the amendments and comments herein.

I. Rejection of Claims 18-21 and 25 Under 35 U.S.C. §102(e)

Claims 18-21 and 25 stand rejected under 35 U.S.C.§102(e) as being anticipated by U.S. Patent No. 6,728,941 to Chen ("Chen"). Withdrawal of this rejection is respectfully requested for at least the following reasons.

Claim 18 has been amended to recite that the means for determining switching power related parameters comprises means for determining crossover current over a plurality of channel connected regions by evaluating predetermined crossover equations with respective crossover current parameters for a given channel connected region over a plurality of channel connected regions, and summing the determined crossover currents to generate a total crossover current. This element was recited in allowable claim 26. Chen does not disclose this element, and therefore does not anticipate claim 18. Claims 19 and 20 depend from claim 18, and therefore are also not anticipated by Chen. Withdrawal of the rejection of claims 18-20 is respectfully requested.

Claim 21 has been amended include the elements from allowable claim 23, which has been cancelled, and now recites the computing at least one leakage power related parameter comprising determining gate tunneling leakage by adding a sum of transistor gate areas of p-type devices multiplied by a predetermined p-type leakage coefficient to a sum of transistor gate areas of n-type devices multiplied by a predetermined n-type leakage coefficient, and determining source-to-drain leakage by adding a sum of transistor gate areas of high voltage threshold (HVT)-type devices multiplied by a predetermined HVT-type leakage coefficient to a sum of transistor gate areas of low voltage threshold (LVT)-type devices multiplied by a predetermined LVT-type leakage coefficient. Chen does not disclose the elements recited in amended claim 21,

and therefore does not anticipate claim 21. Claims 25 depends from claim 21, and therefore is also not anticipated by Chen. Withdrawal of the rejection of claims 21 and 25 is respectfully requested.

II. New Claims 30-42

New claim 30 recites means for determining leakage power related parameters by evaluating predetermined characterizations that functionally relate a second set of circuit design characteristics as a function of leakage power related parameters, the means for determining leakage power determines leakage currents for a plurality of transistor devices by multiplying predetermined leakage coefficients associated with a given transistor type by the sums of transistor gate areas associated with the given type for a plurality of transistor types, and summing the determined leakage currents to generate a total leakage current. New claim 30 incorporates elements from originally examined claims 21 and allowable claim 26. Chen does not disclose the use of predetermine leakage coefficients, as recited in new claim 30. Therefore, new claim 30 should be allowable. New claims 31 and 32 depend from claim 30, and should also be allowable.

New claim 33 recites a power estimation method comprising analyzing the circuit design to determine a switching capacitance characterization, a crossover current characterization and a leakage current characterization associated with the circuit design, and storing the switching capacitance characterization, the crossover current characterization and the leakage current characterization. The method further comprises receiving a plurality of circuit design characteristics associated with a given instance of a circuit design, computing total switching capacitance based on node capacitance of the given instance of the circuit design and the switching capacitance characterization, computing total crossover current based on crossover current parameters of the given instance of the circuit design and the crossover current characterization, computing total leakage current based on transistor gate area of the given instance of the circuit design and the leakage current characterization, and determining total power of the given instance of the circuit design based on the computed total switching capacitance, total crossover current and total leakage current.

Chen does not disclose stored predetermined characterizations for each of crossover current, switching capacitance power and leakage power that can be employed with circuit design characteristics, such as node capacitance, crossover current parameters, and transistor gate area, respectively, to determine power for a given circuit instance. Therefore, claim 33 should be allowable over Chen. New claims 34-42 depend from claim 33, and should also be allowable over Chen.

CONCLUSION

In view of the foregoing remarks, Applicant respectfully submits that the present application is in condition for allowance. Applicant respectfully requests reconsideration of this application and that the application be passed to issue.

Should the Examiner have any questions concerning this paper, the Examiner is invited and encouraged to contact Applicant's undersigned attorney at (216) 621-2234, Ext. 104.

No additional fees should be due for this response. In the event any fees are due in connection with the filing of this document, the Commissioner is authorized to charge those fees to Deposit Account No. 08-2025.

Respectfully submitted,

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